SUBSTITUTE FORM PTO-1390 U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER
12816-027001

U.S. APPLICATION NO. (If Known, see 37 CFR 1.5)
09/914749

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/00655	2 March 2000	2 March 1999

TITLE OF INVENTION
METHOD FOR IMPROVING THERMAL PROCESS STEPS

APPLICANT(S) FOR DO/EO/US
Wilhelm Kegel and Thomas Schuster

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to promptly begin national examination procedures (35 U.S.C. 371(f)).
4. ☐ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is attached hereto (required only if not communicated by the International Bureau).
   b. ☐ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ An English language translation of amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☒ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 16 below concern other documents or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☐ Other items or information:

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Sept. 4 2001 Samantha Bell Samantha Bell

Date of Deposit Signature Typed Name of Person Signing

U.S. APPLICATION NO. (IF KNOWN) 09/914749	INTERNATIONAL APPLICATION NO. PCT/DE00/00655	ATTORNEY'S DOCKET NUMBER 12816-027001

17. ☒ The following fees are submitted:

Basic National Fee (37 CFR 1.492(a)(1)- (5)):

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1000**

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$860**

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO..... **$710**

International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)..... **$690**

International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)..... **$100**

CALCULATIONS PTO USE ONLY	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$860.00
Surcharge of **$130** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$0.00

Claims	Number Filed	Number Extra	Rate		
Total Claims	7 - 20 =	0	x **$18**	$0.00	
Independent Claims	1 - 3 =	0	x **$80**	$0.00	
MULTIPLE DEPENDENT CLAIMS(S) (if applicable)			+ **$270**	$0.00	
TOTAL OF ABOVE CALCULATIONS =				$860.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$0.00	
SUBTOTAL =				$860.00	
Processing fee of **$130** for furnishing the English Translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f))				$0.00	
TOTAL NATIONAL FEE =				$860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$0.00	
TOTAL FEES ENCLOSED =				$860.00	
				Amount to be refunded:	$
				Charged:	$

a. ☒ A check in the amount of $860.00 to cover the above fees is enclosed.
b. ☐ Please charge my Deposit Account No. 06-1050 in the amount of $0.00 to cover the above fees. A duplicate copy of this sheet is enclosed.
c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 06-1050. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b) must be filed and granted to restore the application to pending status.

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REGISTRATION NUMBER

09914749 09/914749

Attorney's Docket No.: 12816-027001 / S1318 sb/FLU

518 Rec'd PCT/PTO 04 SEP 2001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Wilhelm Kegel et al. Art Unit : Unknown
Serial No. : Unassigned Examiner : Unknown
Filed : Herewith
Title : METHOD FOR IMPROVING THERMAL PROCESS STEPS

BOX PCT
Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Prior to examination, please amend the application as follows:

In the specification:

On page 1, line 4, insert:

--FIELD OF INVENTION--

On page 1, line 14, insert:

--BACKGROUND--

On page 1, line 13, insert :

--SUMMARY--

On page 3, line 30, insert:

--DETAILED DESCRIPTION--

On page 5, line 7, insert the new paragraph:

--What we claim as new and secured by letters patent is:--

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September 4, 2001
Date of Deposit

Samantha Bell
Signature

Samantha Bell
Typed or Printed Name of Person Signing Certificate

In the claims:

Please amend claims 1 through 7 as follows:

-- **1.** (**Amended**) A method for improving thermal process steps in the patterning of semiconductor wafers, in particular in rapid thermal processing (RTP) processes preferably during AA oxidation, sacrificial oxidation and GC sidewall oxidation, in which the wafer, in a process chamber, is heated to the process temperature at a predetermined heating rate and, after the envisaged process time has elapsed, is cooled again at a predetermined cooling rate, wherein the wafer is heated at a heating rate of approximately 12°C/sec up to a brief stabilization step at constant temperature and then up to the envisaged process temperature at a heating rate of 10°C/sec and, after the process time has elapsed, is cooled down to room temperature again at a predetermined low cooling rate.

2. (**Amended**) The method as claimed in claim **1**, wherein the stabilization step is raised to a temperature of 120°C below the process temperature.

3. (**Amended**) The method as claimed in claim **2**, wherein the temperature of the stabilization step is 1000°C.

4. (**Amended**) The method as claimed in claim **1**, wherein the wafer is cooled at a cooling rate of approximately 20°C/sec.

5. (**Amended**) The method as claimed in claim **4**, wherein the wafer, at least in the temperature range in which wafer distortions can occur, is cooled at the cooling rate of approximately 20°C/sec from the process temperature to 120° below the process temperature and is then cooled at a lower cooling rate.

6. (**Amended**) The method as claimed in claim **1** wherein a flushing step at the start of the recipe is shortened to an extent such that the process chamber is sufficiently flushed with process gas.

7. (**Amended**) The method as claimed in claim **1** wherein the cooling step at the end of the recipe is set in such a way that the exit temperature from the process chamber is 600°C. --

Please consider additional claims 8-15:

-- **8.** (**New**) A method for controlling temperature of a semiconductor wafer in a process chamber, said method comprising:

heating said chamber from a starting temperature to a stabilizing temperature at a heating rate of approximately 12 degrees Celsius per second;

maintaining said chamber at said stabilizing temperature for a selected stabilization period;

heating said chamber from said stabilizing temperature to a process temperature at a heating rate of approximately 10 degrees Celsius per second;

maintaining said chamber at said process temperature for a selected processing period; and

cooling said chamber from said process temperature to an exit temperature at a selected low cooling rate.

9. (**New**) The method of claim **8**, further comprising selecting said stabilizing temperature to be approximately 89 percent of said process temperature.

10. (**New**) The method of claim **8**, further comprising selecting said stabilizing temperature to be approximately 120 degrees Celsius below said process temperature.

11. (**New**) The method of claim **10**. further comprising selecting said stabilizing temperature to be approximately 1000 degrees Celsius.

12. (**New**) The method of claim **8**, wherein cooling said chamber comprises selecting said cooling rate to be approximately 20 degrees per second.

13. (**New**) The method of claim **8**, wherein cooling said chamber comprises cooling said chamber at a first cooling rate until said chamber is at a critical temperature above which wafer distortions can occur, and cooling said chamber at a second cooling rate between said critical temperature and an exit temperature, said second cooling rate being lower than said first cooling rate.

14. (**New**) The method of claim **8**, wherein cooling said chamber comprises selecting said exit temperature to be approximately 600 degrees Celsius.

15. (**New**) The method of claim **8**, further comprising shortening a flushing step to an extent such that said process chamber is sufficiently flushed with process gas. --

REMARKS

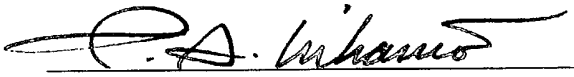
Applicant amends claims 1-7 to remove multiple dependencies and to conform to conventions of U.S. practice. Applicant also presents new claims 8-15 to claim additional aspects of the invention. Applicant amends the specification to conform to conventions of U.S. practice. No new matter is introduced by the foregoing amendments.

Now pending in this application are method claims 1-7 and 8-15, of which claims 1 and 8 are independent.

No additional fees are believed to be due in connection with the filing of this preliminary amendment. However, to the extent that additional fees are due, or if a refund is forthcoming, please adjust our deposit account 06-1050.

Respectfully submitted,

Date: 9/4/01



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20310425 doc

Version with markings to show changes made

In the specification:

Paragraph beginning at page 1, line 1 delete the following:

[Description]

In the claims:

Claims 1 through 7 have been amended as follows:

1. (**Amended**) A method for improving thermal process steps in the patterning of semiconductor wafers, in particular in rapid thermal processing (RTP) processes preferably during AA oxidation, sacrificial oxidation and GC sidewall oxidation, in which the wafer, in a process chamber, is heated to the process temperature at a predetermined heating rate and, after the envisaged process time has elapsed, is cooled again at a predetermined cooling rate, [~~characterized in that~~] wherein the wafer is heated at a heating rate of approximately 12°C/sec up to a brief stabilization step at constant temperature and then up to the envisaged process temperature at a heating rate of 10°C/sec and, after the process time has elapsed, is cooled down to room temperature again at a predetermined low cooling rate.

2. (**Amended**) The method as claimed in claim **1**, [~~characterized in that~~] wherein the stabilization step is raised to a temperature of 120°C below the process temperature.

3. (**Amended**) The method as claimed in claim **2**, [~~characterized in that~~] wherein the temperature of the stabilization step is 1000°C.

4. (**Amended**) The method as claimed in [~~claims 1 to 3~~] claim **1**, [~~characterized in that~~] wherein the wafer is cooled at a cooling rate of approximately 20°C/sec.

5. (**Amended**) The method as claimed in claim **4**, [~~characterized in that~~] wherein the wafer, at least in the temperature range in which wafer distortions can occur, is cooled at the cooling rate of approximately 20°C/sec from the process temperature to 120° below the process temperature and is then cooled at a lower cooling rate.

6. (**Amended**) The method as claimed in claim 1 [~~claims 1 to 5, characterized in that the~~] wherein a flushing step at the start of the recipe is shortened to an extent such that the process chamber is sufficiently flushed with process gas.

7. (**Amended**) The method as claimed in claim 1 [~~claims 1 to 6, characterized in that~~] wherein the cooling step at the end of the recipe is set in such a way that the exit temperature from the process chamber is 600°C.

Description

Method for improving thermal process steps

The invention relates to a method for improving thermal process steps in the patterning of semiconductor wafers, in accordance with the preamble of claim 1, as disclosed in Appl. Phys. A, Vol. A46, No. 4, pp. 255-273, 1988.

The oxides produced in these process steps are used, on the one hand, as screen oxides for the well implantations and, on the other hand, as an intermediate layer for reducing mechanical stress. The oxidation steps take place in a process chamber at relatively high process temperatures, with the result that the wafers are exposed to considerable thermal loading during these process steps, in particular in the case of high heating and cooling rates. The wafers are heated up to a stabilization step at 750°C, for example at 50°C/sec, and then up to the process temperature at a heating rate of 46°C/sec in the case of AA oxidation. The cooling rate may be 50°C/sec in the upper temperature range.

What are problematic are, in particular, the RTP processes in AA oxidation, sacrificial oxidation and in GC sidewall oxidation. The integrated gate stack, in particular, reacts sensitively to high heating rates.

The thermal loading occurring in this case can lead to lateral wafer distortions which result in uncorrectable positional errors of the structure planes lying one above the other, in particular of the contact hole planer. Positional errors

above the other, in particular of the contact hole planes. Positional errors of this type did not occur with the hitherto customary structure widths of significantly more than 0.25 mm and the wafer material used.

With technologies of 0.25 mm for large scale integrated memory components, such positional errors in the contact hole planes, which also lead to DC yield losses, are no longer acceptable and can lead to significant losses of yield or even to the total functional incapability of entire batches.

The invention is therefore based on the object of providing a method for improving thermal process steps in which the disadvantages described above are avoided.

In the case of a method of the type mentioned in the introduction, the formulation of the object on which the invention is based is achieved by virtue of the fact that the wafer is heated at a heating rate of approximately 12°C/sec up to a brief stabilization step at constant temperature and then up to the envisaged process temperature at a heating rate of 10°C/sec and, after the process time has elapsed, is cooled down to room temperature at a predetermined low cooling rate.

The stabilization step is preferably raised to a temperature of 120°C below the process temperature and is 1000°C, for example.

With the reduction of the heating rate and the shifting of the stabilization temperature from hitherto 750°C to 120°C below the process temperature, the temperature response is homogenized over the wafer. As a result, wafer distortions no longer occur.

oxidation processes, i.e. during AA oxidation, sacrificial oxidation and GC sidewall oxidation.

In a continuation of the invention, the wafer is cooled at a cooling rate of approximately 20°C/sec in the high-temperature range. This prevents wafer distortions from being able to occur during cooling.

Preferably, the wafer, at least in the temperature range in which wafer distortions can occur, is cooled at the cooling rate of approximately 20°C/sec from the process temperature to 120° below the process temperature.

Furthermore, it is advantageous if the flushing step at the start of the recipe is reduced to an extent such that the chamber is still sufficiently flushed with process gas and the cooling step at the end of the recipe is reduced to an extent such that the exit temperature is 600°C, with the overall result that the process time is reduced.

The invention will be explained in more detail below using an exemplary embodiment in connection with the figure, a temperature profile for AA oxidation being illustrated in the associated figure of the drawing.

The wafer is heated in a process chamber proceeding from room temperature R at a heating rate of 12°C/sec up to the stabilization step S, which is fixed at 120°C below the process temperature P to be reached, that is to say at 1000°C in the example. The time period of the stabilization step is a few seconds.

Further heating to the process temperature of 1120°C us effected at a heating rate of 10°C/sec.

Raising the stabilization step to 120°C below the process temperature and reducing the heating rates has the

errors in the contact hole planes are at any rate eliminated by the method according to the invention. The consequence is a considerable improvement in the yield and a reduction of the DC yield losses by 7-10%, the outlay concerning the change of recipes of the RTP processes being very low.

Patent Claims

1. A method for improving thermal process steps in the patterning of semiconductor wafers, in which the wafer, in a process chamber, is heated to the process temperature at a predetermined heating rate and, after the envisaged process time has elapsed, is cooled again at a predetermined cooling rate, characterized in that the wafer is heated at a heating rate of approximately 12°C/sec up to a brief stabilization step, with regard to the process duration, at constant temperature and then up to the envisaged process temperature at a heating rate of 10°C/sec and, after the process time has elapsed, is cooled down to room temperature again at a predetermined cooling rate; and in that the stabilization step is raised to a temperature of 120°C below the process temperature.

2. The method as claimed in claim 1, characterized in that the thermal process step is a rapid thermal processing (RTP) process during an oxidation.

3. The method as claimed in claim 1 or 2, characterized in that the temperature of the stabilization step is 1000°C.

4. The method as claimed in one of claims 1 to 3, characterized in that the wafer is cooled at a cooling rate of approximately 20°C/sec.

5. The method as claimed in claim 4, characterized in that the wafer, at least in the temperature range in which wafer distortions can occur, is cooled at the cooling rate of approximately 20°C/sec from the process temperature to 120° below the process

temperature and is then cooled at a lower cooling rate.

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Internationales Buro

INTERNATIONALE ANMELDUNG VERÖFFENTLICHT NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT)

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H01L 21/316	A1	WO 00/52748
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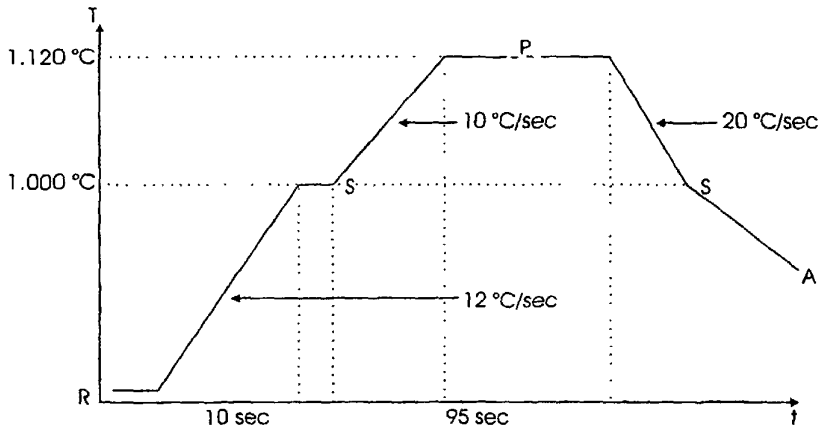
(81) Bestimmungsstaaten: CN, JP, KR, US, europäisches Patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Veröffentlicht
Mit internationalem Recherchenbericht.
Vor Ablauf der für Änderungen der Ansprüche zugelassenen Frist; Veröffentlichung wird wiederholt falls Änderungen eintreffen.

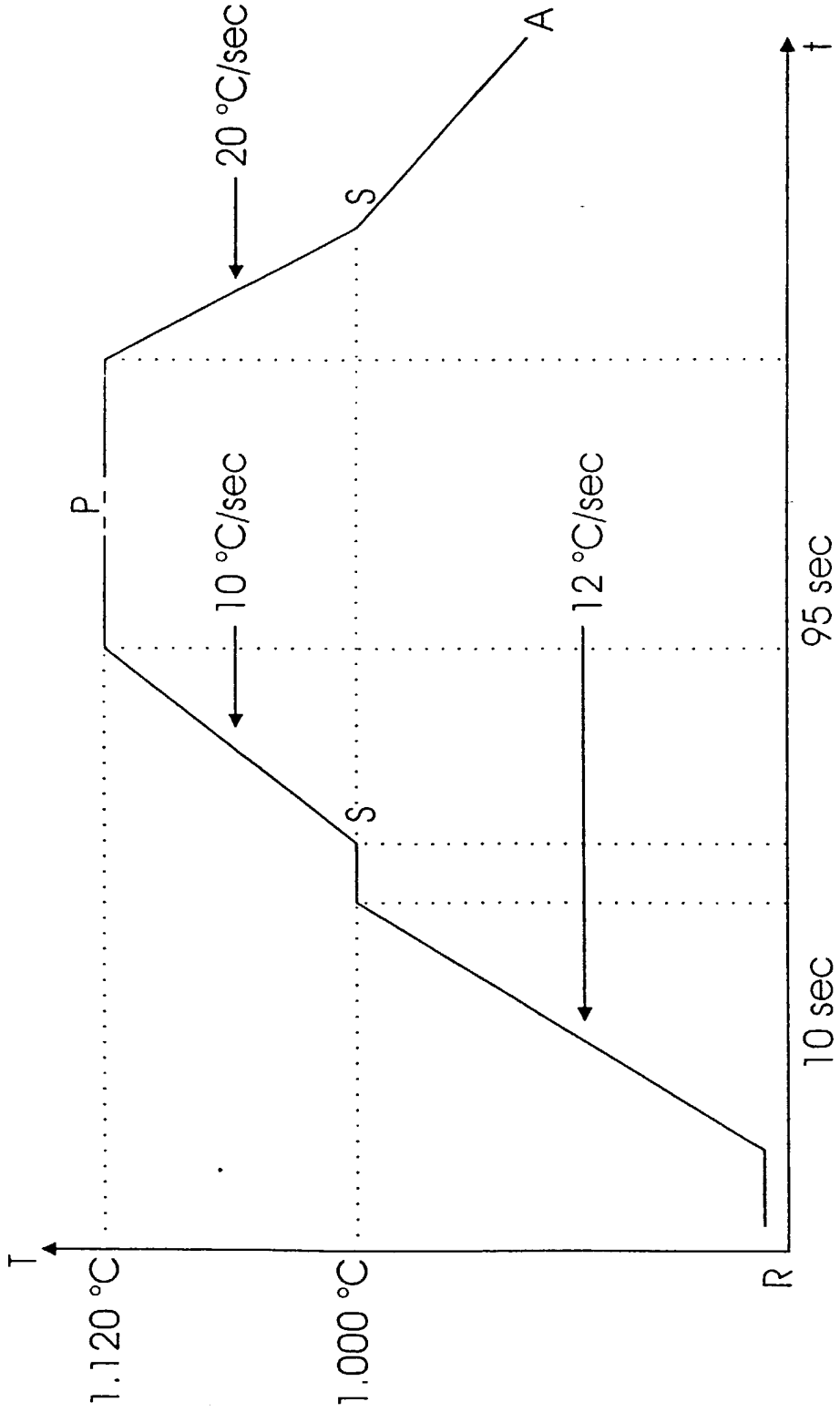
(54) Title: METHOD FOR IMPROVING THERMAL PROCESS STEPS

(54) Bezeichnung: VERFAHREN ZUR VERBESSERUNG THERMISCHER PROZESSSCHRITTE



(57) Abstract

The invention relates to a method for improving thermal process steps, especially in RTP processes during various oxidation processes. The inventive method is characterized in that the wafer is heated with a heating rate of approximately 12 °C/sec until a stabilization step is reached at a temperature of 120 °C below the process temperature and, afterwards, is heated with a heating rate of 10 °C/sec until a process temperature is obtained. The wafer is then cooled with a lower cooling rate of approximately 20 °C/sec down to the exit temperature.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10 sec

Attorney's Docket No.: 12816-027001
Client's Ref. No.: S1318 sb/FLU

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled METHOD FOR IMPROVING THERMAL PROCESS STEPS, the specification of which:

[] is attached hereto.
[X] was filed on September 4, 2001 as Application Serial No. 09/914,749 and was amended on _____.
[] was described and claimed in PCT International Application No. PCT/DE00/00655 filed on 03/02/00 and as amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

(2) Frank R. Occhiuti, Reg. No. 35,306 Faustino A. Lichauco, Reg. No. 41,942

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

1-00

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Combined Declaration and Power of Attorney

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